of the photodiode detector and including a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown.

2. *(Amended)* A photodetector circuit according to Claim 1 wherein the CMOS component comprises a substrate supporting and insulated from said CMOS circuitry, the photodiode detector is operable in current multiplication mode and the at least one epitaxial layer is deposited upon the substrate.

3. *(Amended)* A photodetector circuit according to Claim 39, wherein the at least one epitaxial layer provides a high field region.

4. *(Amended)* A photodetector circuit according to Claim 2 wherein the photodiode detector is an avalanche photodiode and said photodiode comprises a first region incorporated in the substrate, and the at least one epitaxial layer is a layer upon the first region and provides a second region of the photodiode.

5. *(Amended)* A photodetector circuit according to Claim 2, wherein the at least one epitaxial layer comprises two layers providing second and third regions of the photodiode, the second region is upon the first region and the third region is upon the second region, the first and third regions are of mutually opposite conductivity type, the second region is substantially undoped and the third region is an epitaxial layer.

6. (*Amended)* A photodetector circuit according to Claim 5,wherein in that the third avalanche photodiode region is electrically connected to the guard ring and has like potential therewith during circuit operation

7. (*Amended)* A photodetector circuit according to Claim 1 arranged to provide a logarithmic response to incident radiation.

8. (*Amended)* A photodetector circuit according to Claim 1, wherein said circuit incorporates parasitic photodiodes arranged to contribute to circuit output in response to incident radiation.

9. (*Amended)* A photodetector circuit according to Claim 1, wherein said circuit includes an amplifier arranged to provide feedback to stabilise photodiode detector bias voltage.

10. (*Amended)* A photodetector circuit according to Claim 9, wherein the amplifier is arranged to amplify an output signal from the photodiode detector and to provide feedback to bias a load transistor (ML5) in series with the photodiode detector.

11. (*Amended)* A photodetector circuit according to Claim 10, wherein the amplifier is a push-pull amplifier.

12. (*Amended)* A photodetector circuit according to Claim 10, wherein said circuit includes a cascode transistor arranged to reduce Miller Effect capacitance

in the amplifier.

13. *(Amended)* A photodetector circuit according to Claim 1, wherein the CMOS component is a substrate supporting and insulated from CMOS circuitry, the photodiode detector comprises a first region of one conductivity type incorporated in the substrate, the at least one epitaxial layer comprises two epitaxial layers one of which is substantially undoped and the other of which is of opposite conductivity type to that of the first region, the first region and the two epitaxial layers being configured as a PIN diode.

14. *(Amended)* A photodetector circuit according to Claim 13, wherein the undoped epitaxial layer is of SiGe alloy or is a quantum well structure of the $Si_{1-x}Ge_x$ material system where the value of the compositional parameter x changes between successive layers.

--38. *(New)* A photodetector circuit comprising:

a photodiode detector, said photodetector having a PIN structure, said structure having three active regions, one region p-type, one region substantially undoped and one region n-type; and

an associated readout circuit, said circuit incorporates a CMOS component supporting at least one deposited epitaxial layer which is one of said active regions of the photodiode detector and including a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown.

39. *(New)* A photodetector circuit according to Claim 38 wherein the CMOS component comprises a substrate supporting and insulated from said CMOS circuitry, the photodiode detector is operable in current multiplication mode and the at least one epitaxial layer is deposited upon the substrate.

40. *(New)* A photodetector circuit according to Claim 39, wherein the photodiode detector is an avalanche photodiode and said photodiode comprises a first region incorporated in the substrate, and the at least one epitaxial layer is a layer upon the first region and provides a second region of the photodiode.

41. *(New)* A photodetector circuit according to Claim 39, wherein the at least one epitaxial layer comprises two layers providing second and third regions of the photodiode, the second region is upon the first region and the third region is upon the second region, the first and third regions are of mutually opposite conductivity type, the second region is substantially undoped and the third region is an epitaxial layer.

42. *(New)* A photodetector circuit according to Claim 41, wherein the third avalanche photodiode region is electrically connected to the guard ring and has like potential therewith during circuit operation.

43. *(New)* A photodetector circuit according to Claim 38, arranged to provide a logarithmic response to incident radiation.

44. *(New)* A photodetector circuit according to Claim 38, wherein said

circuit incorporates parasitic photodiodes arranged to contribute to circuit output in response to incident radiation.

45. *(New)* A photodetector circuit according to Claim 38, wherein said circuit includes an amplifier arranged to provide feedback to stabilise photodiode detector bias voltage.

46. *(New)* A photodetector circuit according to Claim 45, wherein the amplifier is arranged to amplify an output signal from the photodiode detector and to provide feedback to bias a load transistor in series with the photodiode detector.

47. *(New)* A photodetector circuit according to Claim 46, wherein the amplifier is a push-pull amplifier.

48. *(New)* A photodetector circuit according to Claim 46, wherein said circuit includes a cascode transistor arranged to reduce Miller Effect capacitance in the amplifier.

49. *(New)* A photodetector circuit according to Claim 38, wherein the CMOS component is a substrate supporting and insulated from CMOS circuitry, the photodiode detector comprises a first region of one conductivity type incorporated in the substrate, the at least one epitaxial layer comprises two epitaxial layers one of which is substantially undoped and the other of which is of opposite conductivity type to that of the first region, the first region and the two epitaxial layers being configured as a PIN diode.

50. *(New)* A photodetector circuit according to Claim 49, wherein the undoped epitaxial layer is of SiGe alloy or is a quantum well structure of the $Si_{1-x}Ge_x$ material system where the value of the compositional parameter x changes between successive layers.--